THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 26

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte ROBERT M. CHAPIN, KENNETH D. ROMANO,
BENJAMIN D. BROWN, ANTHONY M. FRUMUSA
and PHILLIP A. SCIUTO

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Appeal No. 95-3912
Application 08/087,247[1]

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ON BRIEF

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Before THOMAS, KRASS and TORCZON, Administrative Patent Judges.

THOMAS, Administrative Patent Judge.

DECISION ON APPEAL

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[1] Application for patent filed July 7, 1993.

Appellants have appealed to the Board from the examiner's final rejection of claims 1 to 23, which constitute all the claims in the application.

Representative claim 1 is reproduced below:

1. A chain interface controller for controlling a plurality of integrated input/output controllers, wherein the requirement for a dedicated programmed microprocessor for handling data conversion for said chain interface controller is removed, said chain interface controller comprising:

oversampling means for eliminating random voltage spikes from an input chain of digital data, the input chain comprising a plurality of bits, each bit of said plurality of bits corresponding to an integrated input/output controller and representative of a state of said corresponding integrated input/output controller, said oversampling means eliminating random voltage spikes on said input data chain by sampling each bit of said chain of digital data on a bit-by-bit basis three times during a clock period of the chain of data, each sample being taken at a first predetermined interval from an immediately previous sample, said oversampling means outputting a binary value of each bit of said chain of data, said binary value being representative of a majority of three samples of each bit taken during the clock period, said binary value being an oversampled bit of said chain of digital data;

filter means for debouncing said input chain of digital data by receiving said oversampled bits of data from said oversampling means and filtering each of said oversampled bits three times at a second predetermined interval and storing a filtered sample representative of three successive non-changing samples in a filtered input register, said second predetermined interval being representative of a frame clock period;

input data change detecting means for detecting a change in any bit of the chain of data and changing a status bit of

the input data chain, said status bit indicating a change of state of any bit of the input data chain;

interrupt signal generating means generating an interrupt signal when one bit of the input data chain has changed state, said interrupt signal being transmitted to a host microprocessor, said host microprocessor locating and reading said filtered sample upon the receipt of said interrupt signal;

a serial output data line for transmitting said input chain of digital data to said oversampling means from said plurality of integrated input/output controllers; and

a serial input data line for transmitting an output chain of digital data, said output chain of digital data being a serialized version of parallel output data generated by said host microprocessor for providing instructions to said integrated input/output controllers.

The following references are relied on by the examiner:

Fisk et al. (Fisk)	4,120,034	Oct. 10, 1978
Daughton et al. (Daughton)	4,266,294	May 05, 1981
Federico et al. (Federico)	4,550,382	Oct. 29, 1985

Claims 1 to 23 stand rejected under 35 U.S.C. § 103. As evidence of obviousness, the examiner relies upon Fisk in view of Federico as to claims 1, 3 to 9, 11, 13, 14 and 16 to 23, with the addition of Daughton as to claims 2, 10, 12 and 15.[2]

[2] A rejection of one claim under the second paragraph of 35 U.S.C. § 112 is not repeated in the answer from the final

Rather than repeat the positions of the appellants and the examiner, reference is made to the brief and the answer for the respective details thereof.

OPINION

We reverse the rejections of claims 1 to 23 under 35 U.S.C. § 103.

At the outset, we are not convinced that the examiner has established a prima facie case of obviousness of the claimed invention since, initially, we find that it would not have been obvious for the artisan to have combined from a computer architecture point of view the systems of Fisk and Federico. Various portions of Fisk, for example, indicate various tradeoffs known in the art between a hardware-oriented, control logic based system versus a programmable controller-type approach. Note col. 1 generally of Fisk; col. 11, lines 31 through 54; and col. 18, lines 22 through 38. While Fisk uses a single processor, Federico takes an intermediate architectural design approach by utilizing a master processor to control various subsidiary or discrete processors, which in

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rejection, apparently in view of the filing of an amendment after final which has been entered by the examiner.

turn control individual portions of a photocopying machine. This is a more distributed processing-type architectural approach. In this respect, Federico is more like appellants' broad concept of the disclosure set forth in Fig. 2 of the drawings. The examiner offers us no persuasive line of reasoning as to why the artisan would have found it obvious to combine the teachings into a single system of the two references relied upon.

Assuming for the sake of argument, however, that it would have been obvious for the artisan for some reason to have combined the teachings of Fisk and Federico, we are not convinced that the portions relied upon of the two references the examiner makes reference to would have made obvious the subject matter of at least the independent claims 1, 7, 14 and 20 on appeal. The examiner's approach is to indicate that certain portions of representative claim 1, for example, are found in Fisk and that certain portions of this claim are found in Federico. The examiner's approach is to identify only concepts which appear to be present to the examiner in each of the respective references that are set forth in the claims in a rather detailed format such as the details of the

long oversampling means sub-clause in representative claim 1 on appeal. Both oversampling for a noise immunity purposes and switch debounce immunity are discussed at col. 19 and 20 of Fisk as indicated by the examiner. However, the details of the oversampling and filter means clauses of claim 1 on appeal are not specifically identified by the examiner to be found at this location of the reference and we can find none ourselves. The emphasis in Fisk is noise immunity by oversampling and switch debounce being preformed in a software-oriented approach in the single controller in such a manner as to avoid the need for complex circuits or switches. Because Fisk is computer-based, the artisan would have surmised that the computer was interruptible. However, the interrelationship of the input data change detecting means and the interrupt signal generating means in representative independent claim 1 on appeal go well beyond a general concept of such an interrupt capability existing in prior art microprocessors.

As to independent claim 7, we are not persuaded that the

examiner has provided evidence to us of the three respective predetermined time intervals recited in this claim, that the comparing step as well as the interrupt generation feature occur in the combined teachings of the references in the detail presented. The examiner's position recognizes at the top of page 5 of the answer that Fisk does not need a conversion from serial to parallel data and vice versa since the controller only receives and uses one bit at a time. On the other hand, Federico's shared communication line 80, often referred to by the examiner in the rejection, is an Ethernet-based communication system, which suggests only a serial link. The examiner's arguments make reference to the admitted prior art Fig. 1 of the disclosed invention making reference to serial input data and serial output data, but presents no reasoning as to why the artisan would have utilized such teachings in addition to the combined disparate teachings the examiner has found and shown to exist in Fisk and Federico respectively.

As to independent claims 14 and 20 on appeal, initially we note that claim 20 recites a plurality of the individual chain interface controllers in the same amount of detail that

only a single one of which is recited in independent claim 14. However, these claims recite specific electronic circuit elements known in the art. We are at a loss to determine where such specifically identified elements are to be found in the applied prior art since the detail of which is not specified in them or, as in Federico's or Fisk's approaches, are only software-based. Again, Fisk himself emphasizes the software approach as a preferred tradeoff over the more discrete hardware circuit element approach of circuit design for control and sampling purposes. The claims go well beyond a general assertion of equivalence between hardware and software approaches.

Overall, we are not convinced that the artisan would have found it obvious within 35 U.S.C. § 103 to have combined the respective teachings of Federico and Fisk in the manner argued by the examiner, and even if such would have been obvious to do, we are not convinced that the respective teachings and showings and suggestions in these references meet the features recited in each independent claim on appeal. To some extent there is merit to appellants' argument that the examiner has exercised prohibited hindsight and has picked and chosen bits

and pieces of the respective circuit elements from the respective references relied upon. In any event, we are not convinced the examiner has established a prima facie case of obviousness of the subject matter of independent claims 1, 7, 14 and 20 on the basis of Fisk and Federico. As such, we also reverse the rejection of additional dependent claims further relying upon the teachings of Daughton.

Therefore, the decision of the examiner rejecting claims 1 to 23 on appeal is reversed.

REVERSED

JAMES D. THOMAS Administrative Patent Judge	)
ERROL A. KRASS Administrative Patent Judge	) BOARD OF PATENT) APPEALS AND) INTERFERENCES

RICHARD TORCZON)
Administrative Patent Judge)

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